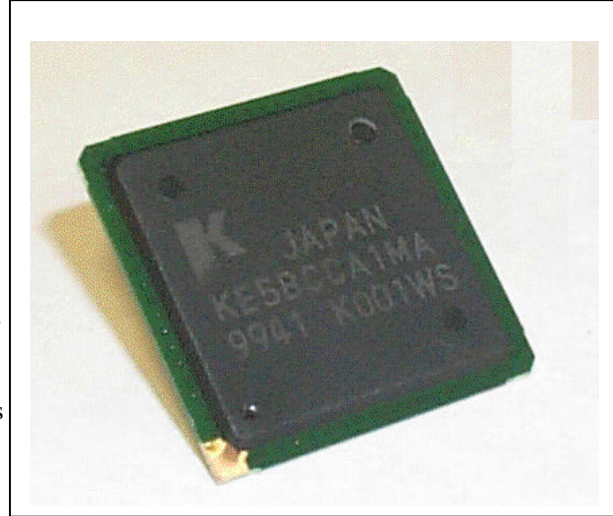


**KE5BCCA1M****Classification CAM**

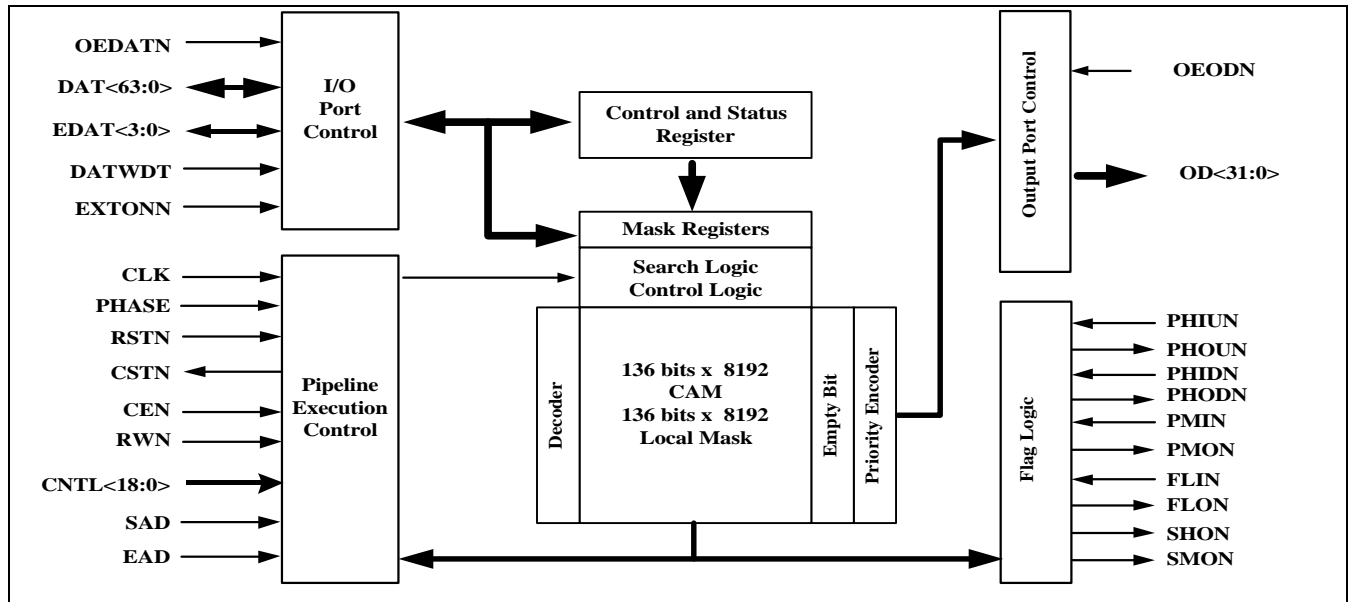
Kawasaki LSI's Classification CAM has a capacity of 1Mbit (Ternary) and 2 Mbit (Binary), and can be configured by bank in a mixture of binary and ternary modes. Its primary application is in search and filtering. Its flexibility, high speed, and high capacity make it appropriate for all Layer 2/3/4 and above applications such as switches and routers in 10/100/1000 Ethernet, Terabit Ethernet, OC-3/12/48/192, T1/T3, frame relay, ATM, xDSL and DWDM.

This Classification CAM is also suitable for QoS applications with its unique and patent-pending "Auto Shift" commands.

The search time is 15ns and the KE5BCCA1M is available in a 324-pin BGA.

**FEATURES:**

- High density: 2Mbits Binary, 1Mbit for Ternary
- Organization: Configurable table width; binary/ternary selected by bank
- Binary case: 68-bit x 32k, 136-bit x 16k, 272-bit x 8k
- Ternary case: 68-bit x 16k, 136-bit x 8k, 272-bit x 4k
- High Speed Search :15n sec (1 phase clock)
- Latency: 30n sec (2 clock cycles)
- Dual-Port Architecture: 68-bit I/O port with
 1. 64-bit data bus (optional 32-bit configuration)
 2. Optional 4 extra bits on the data bus
 3. 32-bit output port
- Cascadable up to 32 pieces
- Support for automatic data shifting
- Continuous search during data shifting.
- Multi-hit support (highest hit address output)
- 18 Global MASK Registers (68-bit width) for data search/writing operation.
- Automatic learning
- Automatic storing of miss-hit data and time stamp of hit data
- Synchronous operation
- Clock rate: 66MHz (phase clock)/133MHz (operating clock) for synchronous operation
- 324-pin BGA packaging
- 2.5V/3.3V power supply

**Kawasaki LSI USA, Inc.**

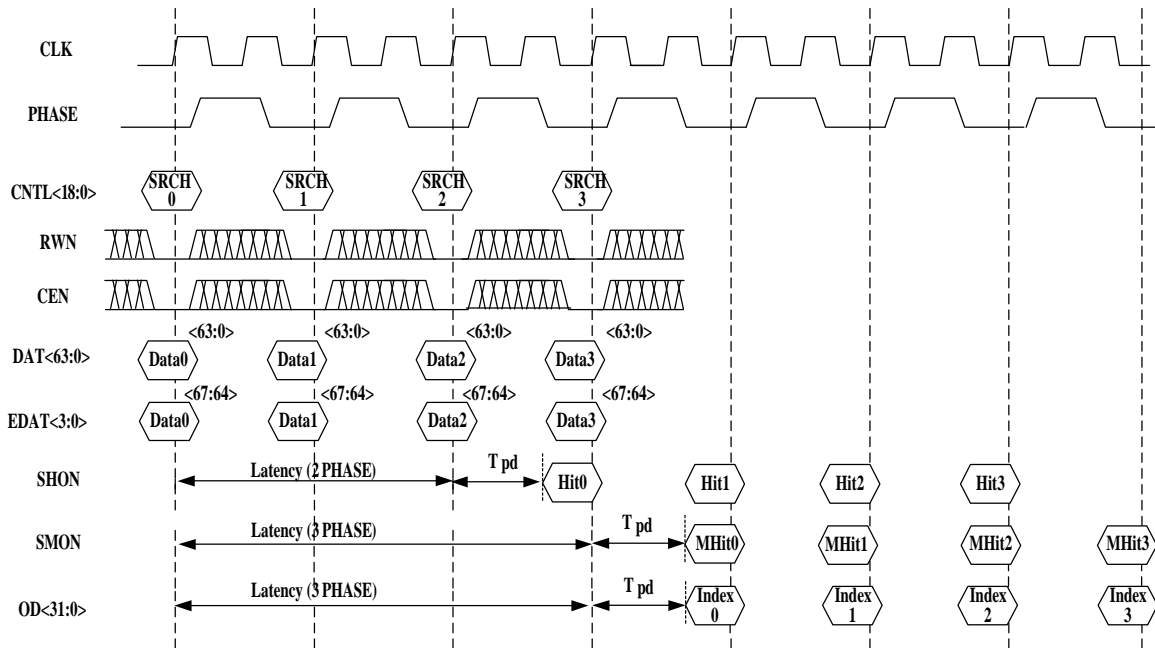
Silicon Valley Office: 2570 North First Street, Suite 301
San Jose, CA 95131
Tel: (408) 570-0555
Fax: (408) 570-0567

www.klsi.com

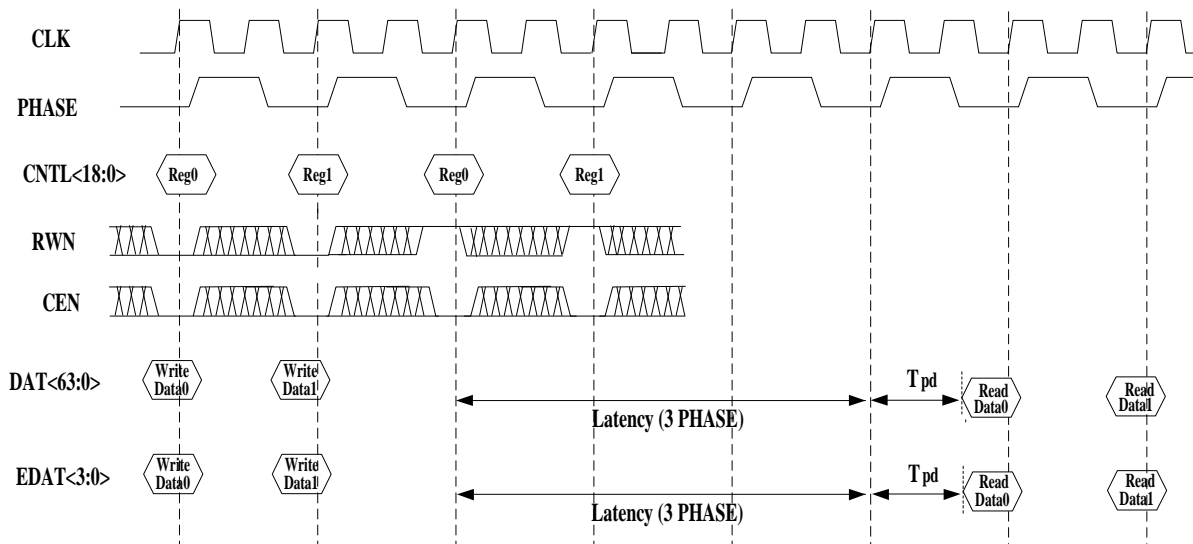
Eastern Office: 501 Edgewater Dr., Suite 510
Wakefield, MA 01880
Tel: (781) 224-4201
Fax: (781) 224-2501

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Timing Chart of Search Operation (68bit)



Timing Chart of Read/Write Operation (68bit)



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